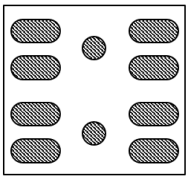
SZCJ Shenzhen Changji Semiconductor Co., LTD.

CSP Enhancement Mode Power MOSFET

CJ8218SP Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	2.2mΩ@4.5V	13.5A
	2.3mΩ@3.8V	
	2.8mΩ@3.1V	
	3.6mΩ@2.5V	

CSPC2019-10



DESCRIPTION

The CJ8218SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment

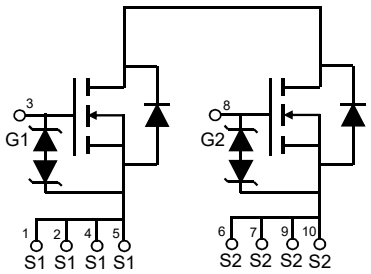


Top View Bottom View

Marking:
1. 8218: Product Code
2. YYMMX: Date Code
3. Solid dot: Pin 1

1,2,4,5. Source1
6,7,9,10. Source2
3. Gate1
8. Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S ①	13.5	A
Source Current (Pulsed)	I_{SP} ①②	135	A
Total Power Dissipation	P_T ①	1.4	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

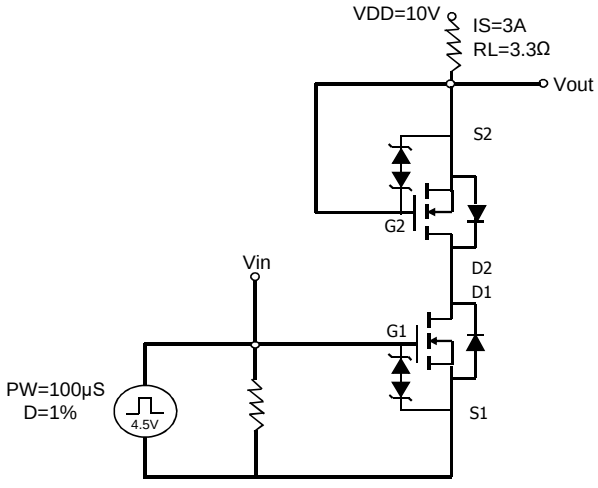
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V,V_{GS}=0V			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V, V_{GS}= ±5V			±1	μA
		V_{SS}=0V, V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage	V_{TH}	V_{SS}=10V, I_{GS}=250uA	0.35	0.80	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=3A	1.2	2.2	2.9	mΩ
		V_{GS}=3.8V,I_S=3A	1.3	2.3	3.0	mΩ
		V_{GS}=3.1V,I_S=3A	1.4	2.8	4.2	mΩ
		V_{GS}=2.5V,I_S=3A	1.8	3.6	6.0	mΩ
Input Capacitance	Ciss	V_{SS}=10V, V_{GS}=0V,f=100kHZ		1373		pF
Output Capacitance	Coss			615		pF
Reverse Transfer Capacitance	Crss			267		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=10V,R_L=3.3Ω V_{GS}=4.5V		0.5		μS
Turn-on Rise Time	t_r ③			2.5		μS
Turn-off Delay Time	$t_{d(off)}$ ③			6.4		μS
Turn-off Fall Time	t_f ③			14.5		μS
Total Gate Charge	Q_g ③	V_{SS}=10V,I_S=6A,V_{GS}=4.5V		36		nC
Gate1-source1 charge	Q_{g1s1} ③			3.6		nC
Gate1-source2 charge	Q_{g1s2} ③			15		nC
Diode Forward Voltage	$V_{F(S-S)}$ ④	V_{SS}=0V,I_S=6.8A			1.3	V

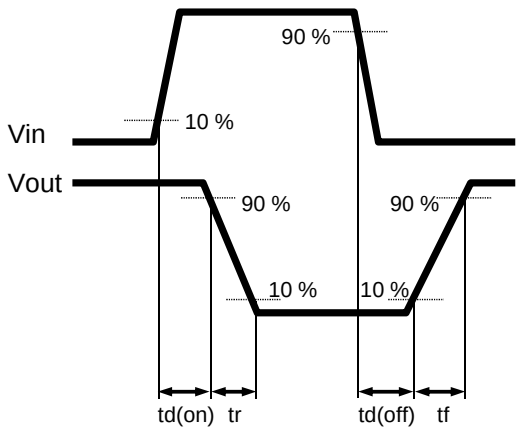
Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using the minimum recommended pad size (36um Copper).

2.t = 10 ms , Duty Cycle = 1 %.

3.When FET1 is measured,G2 and S2 are short-circuited.

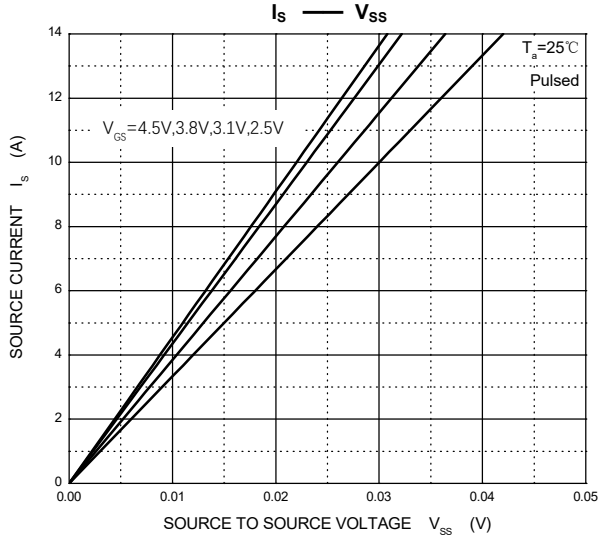
4.When FET1 is measured, FET2 is biased with V_{G2S2}=4.5V.



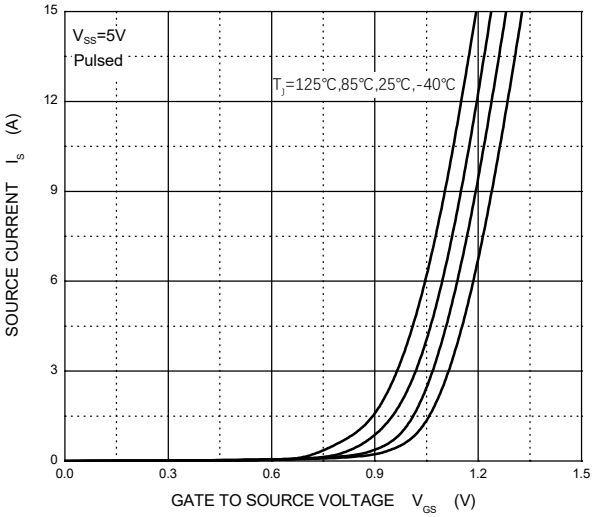


Typical Characteristics

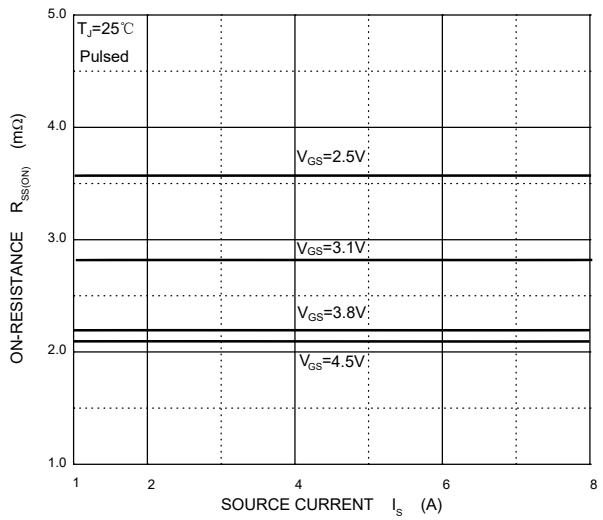
I_S — V_{SS}



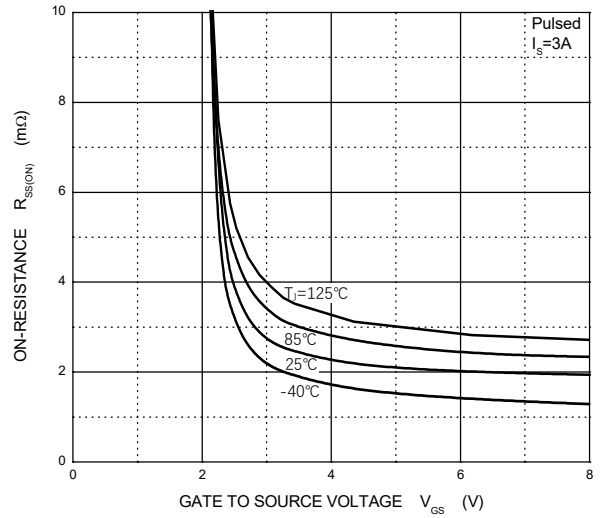
I_S — V_{GS}



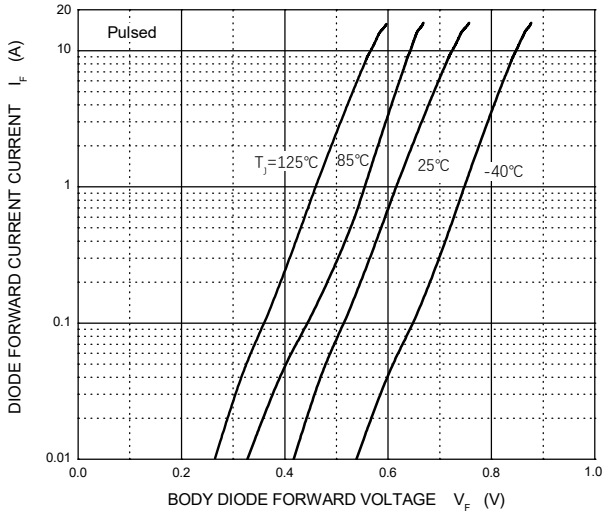
$R_{SS(ON)}$ — I_S



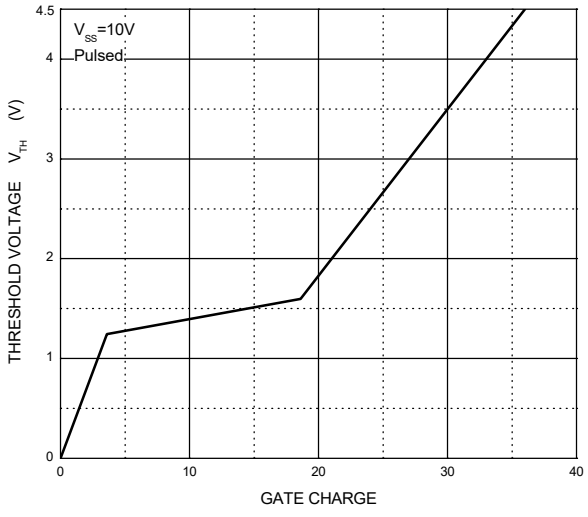
$R_{SS(ON)}$ — V_{GS}



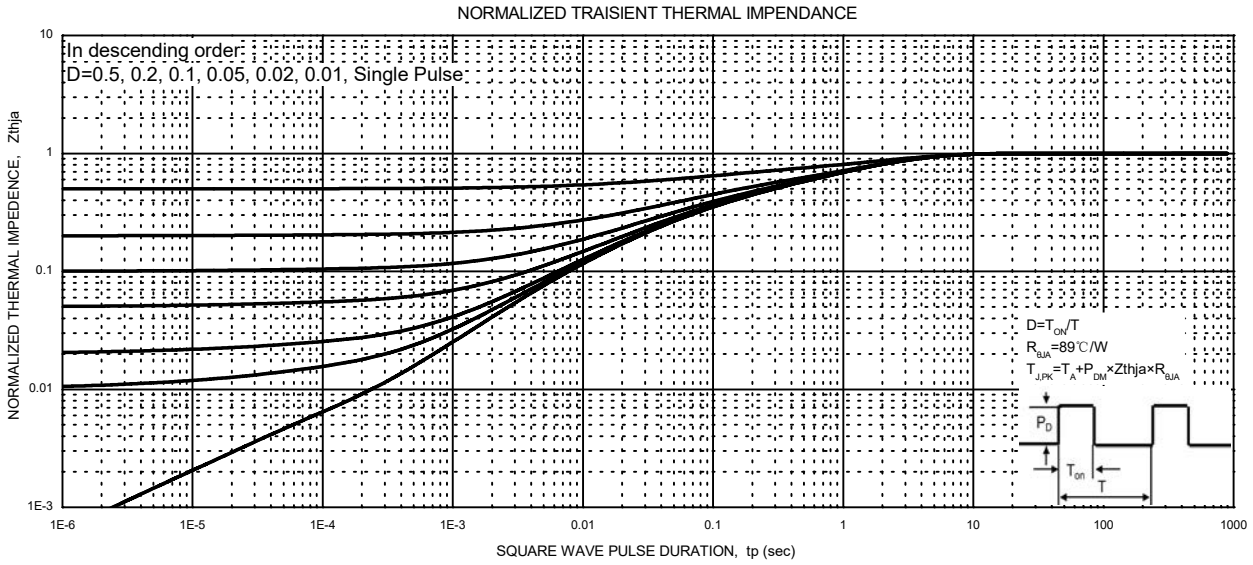
I_F — V_F

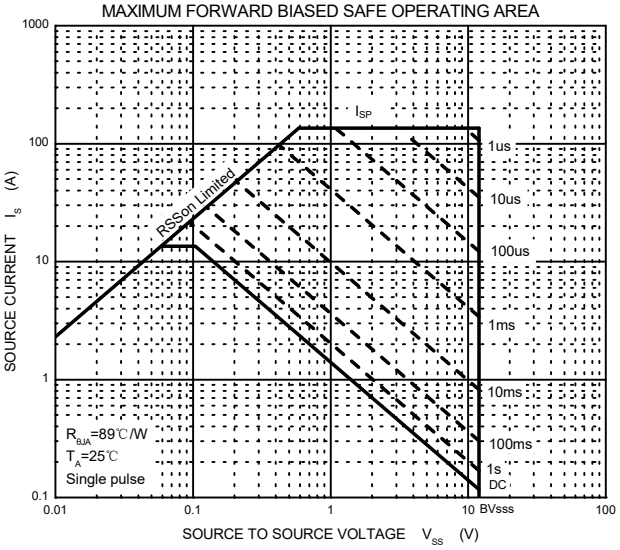


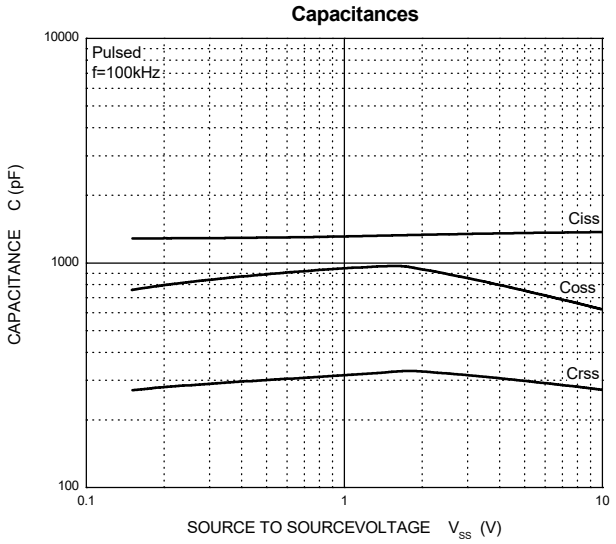
Gate Charge



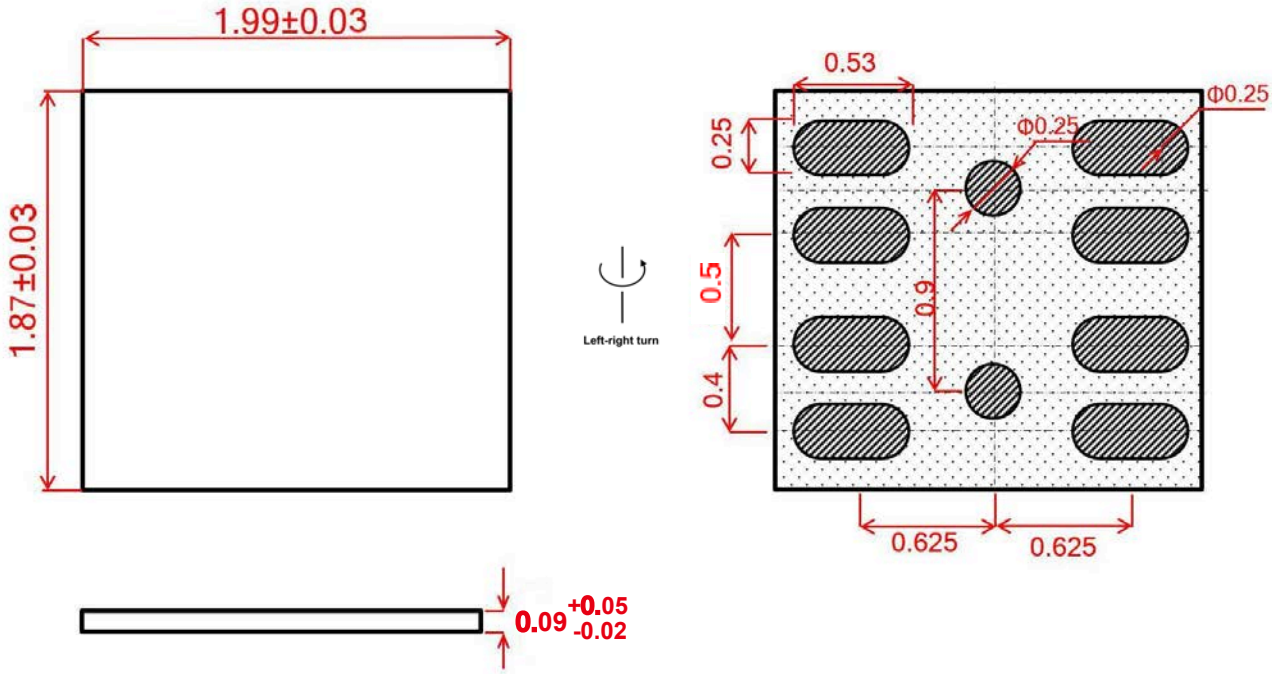
Typical Characteristics



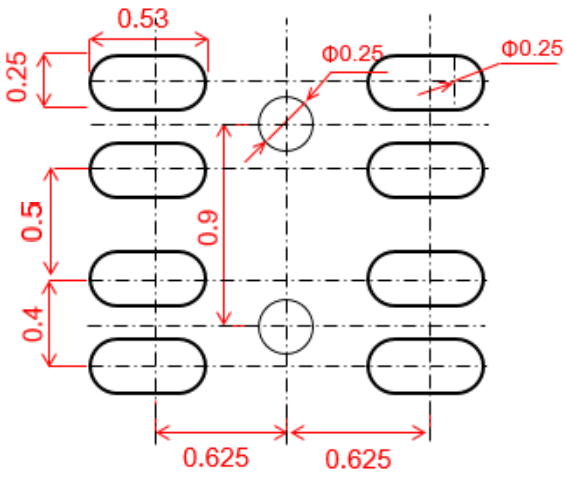




CSPC2019-10 Package Outline Dimensions(Unit:mm)



CSPC2019-10 Suggested Pad Layout (Unit:mm)

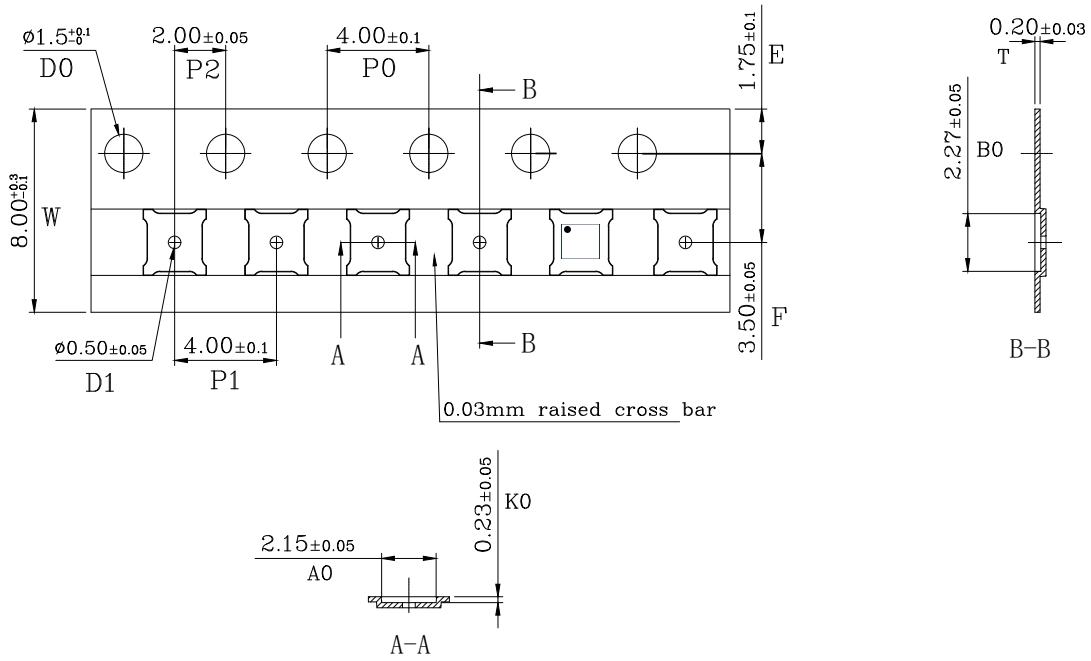


Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

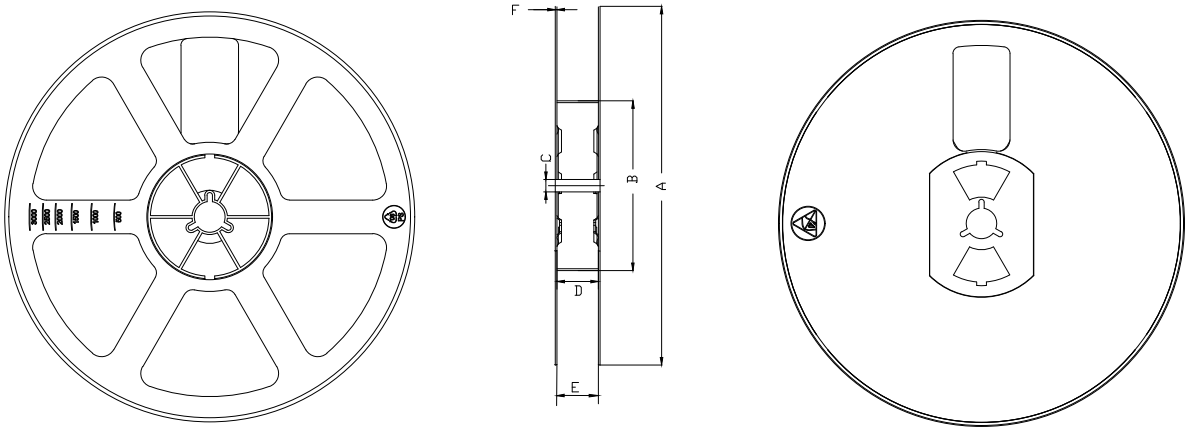
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Tape and Reel



产品尺寸规格 (UNIT:mm)						
规格	A0	B0	K0	P0	P1	P2
尺寸	2.51±0.05	2.72±0.05	0.23±0.05	4.0±0.1	4.0±0.1	2.0±0.05
规格	T	E	F	D0	D1	W
尺寸	0.2±0.03	1.75±0.1	3.5±0.05	$1.5^{+0.1}_{-0.0}$	0.5±0.05	$8.0^{+0.3}_{-0.1}$



SIZE	8MM
A	178±2.0
B	55±1.0
C	$13.0^{+0.35}_{-0.15}$
D	$8.4^{+2.5}_{-0.4}$
E	$8.65^{+4.7}_{-0.65}$
F	1.5±0.5

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