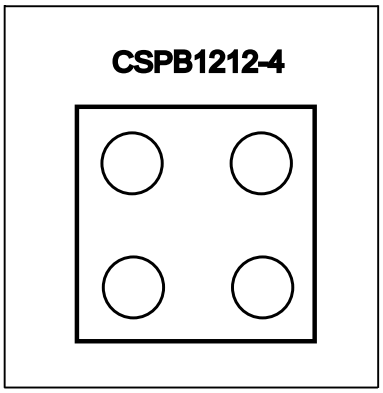
CSP Enhancement Mode Power MOSFET

CJ12025SP Dual N-Channel MOSFET

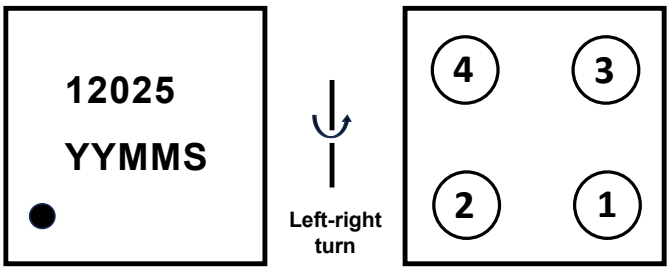
V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	8.2mΩ@4.5V	7.5A
	8.9mΩ@3.8V	
	9.9mΩ@3.1V	
	11.8mΩ@2.5V	



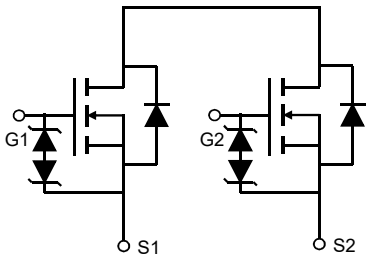
DESCRIPTION

The CJ12025SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment



Equivalent Circuit



Marking:

1. 12025: Product Code
2. YYMMS: Date Code
3. Solid dot: Pin 1

1 Source1 2 Gate1
3 Source2 4 Gate2

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

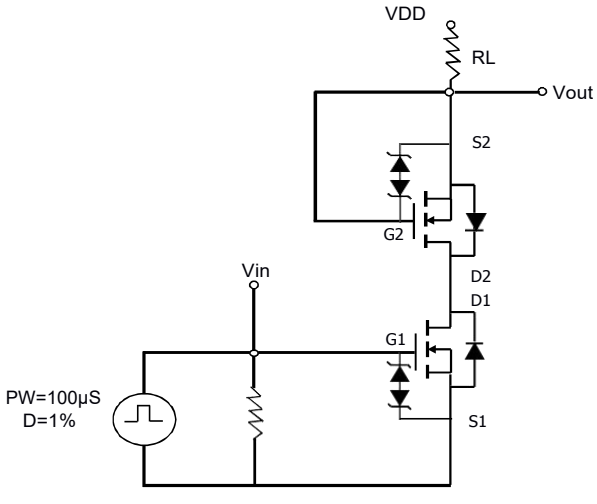
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current (DC)	I_S ①	7.5	A
Source Current (Pulsed)	I_{SP} ①②	75	A
Total Power Dissipation	P_T ①	0.9	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

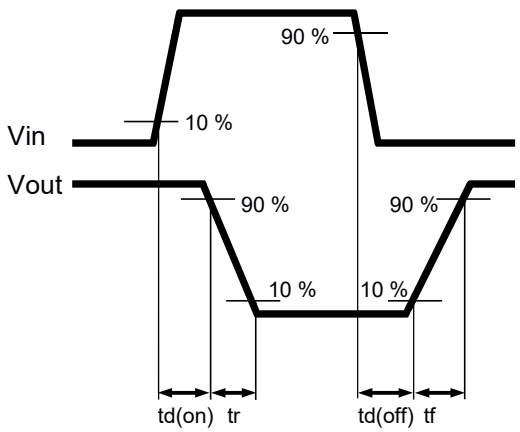
MOSFET ELECTRICAL CHARACTERISTICS

T_a=25 ℃ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=12V,V_{GS}=0V			1.0	μA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V, V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=6V, I_S=250μA	0.5	0.9	1.3	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=2A	6.0	8.2	10.0	mΩ
		V_{GS}=3.8V,I_S=2A	6.2	8.9	11.5	mΩ
		V_{GS}=3.1V,I_S=2A	6.9	9.9	13.5	mΩ
		V_{GS}=2.5V,I_S=2A	8.2	11.8	17	mΩ
Gate resistance	R_g ③	f=1MHz		550		Ω
Input Capacitance	Ciss	V_{SS}=10V, V_{GS}=0V,f=1kHZ		727		pF
Output Capacitance	Coss			184		pF
Reverse Transfer Capacitance	Crss			137		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=6V,R_L=1.5Ω, V_{GS}=4.5V		176		nS
Turn-on Rise Time	t_r ③			337		nS
Turn-off Delay Time	$t_{d(off)}$ ③			1053		nS
Turn-off Fall Time	t_f ③			727		nS
Total Gate Charge	Q_g ③	V_{SS}=6V,I_S=7.5A,V_{GS}=4.5V		8.0		nC
Gate1-source1 charge	Q_{g1s1} ③			1.4		nC
Gate1-source2 charge	Q_{g1s2} ③			2.2		nC
Diode Forward Voltage	$V_{F(S-S)}$	V_{GS}=0V,I_S=2A			1.0	V

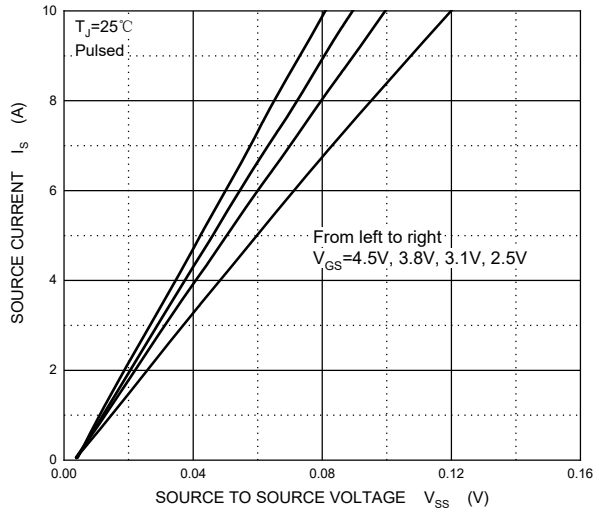
Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using the minimum recommended pad size (36um Copper).
2.t = 10 us , Duty Cycle = 1 %.
3.When FET1 is measured,G2 and S2 are short-circuited.



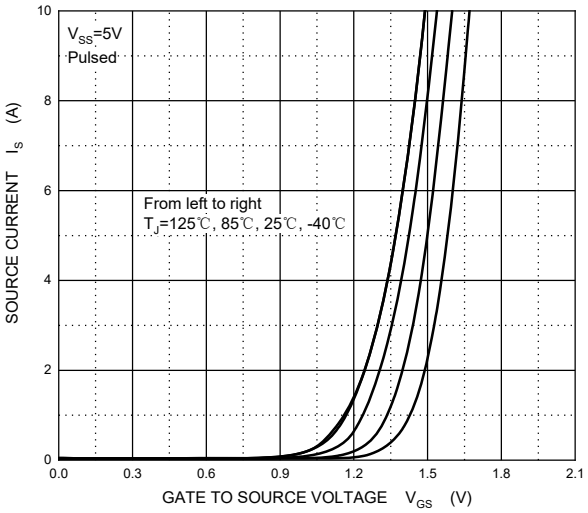


Typical Characteristics

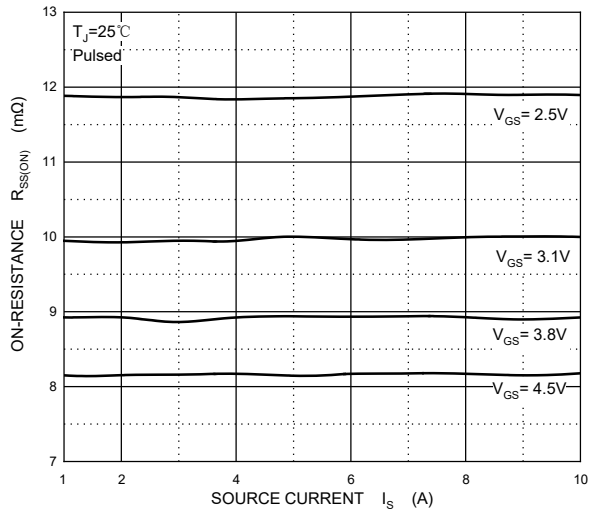
I_S—V_{SS}



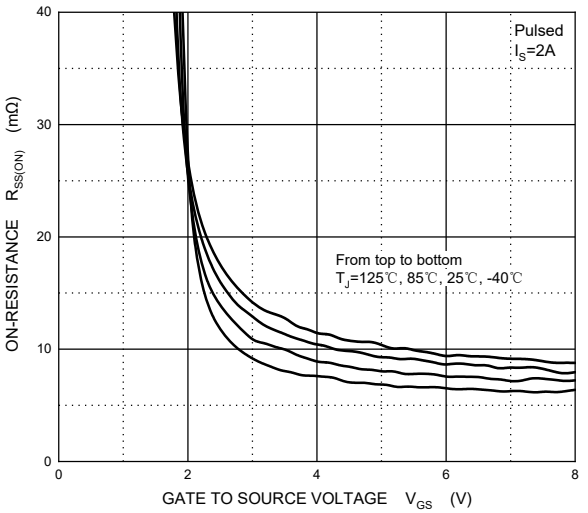
I_S—V_{GS}



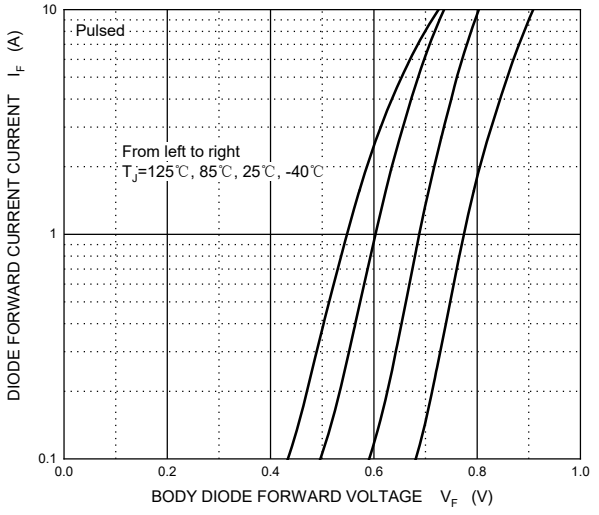
$R_{SS(ON)}$—I_S



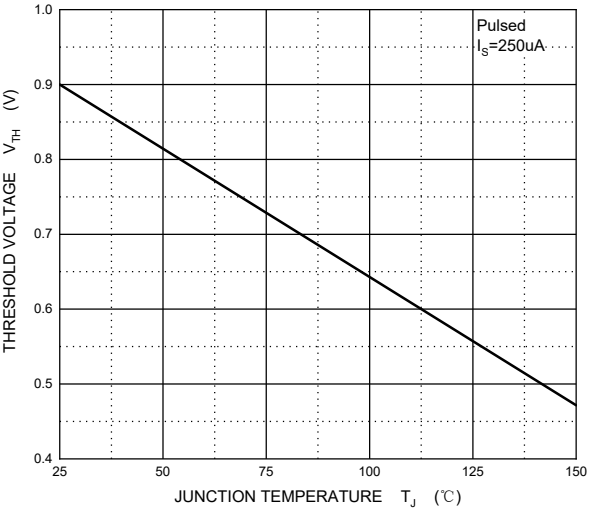
$R_{SS(ON)}$—V_{GS}



I_F—V_F

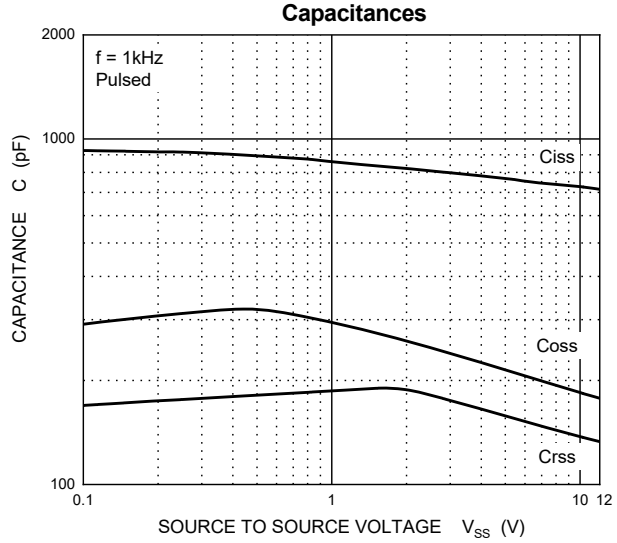


Threshold Voltage

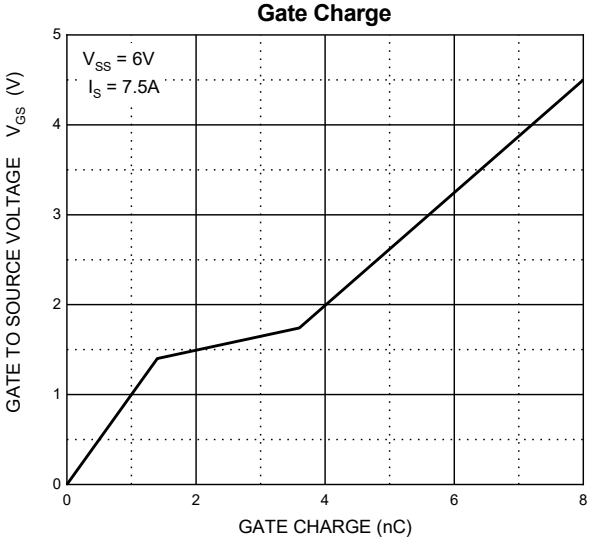


Typical Characteristics

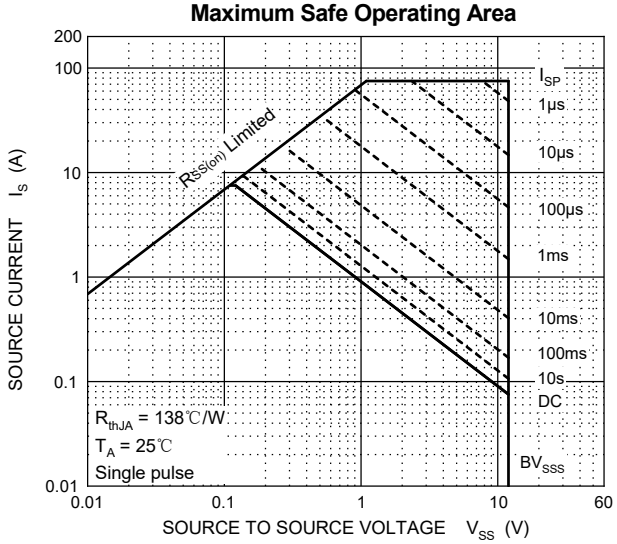
Capacitances



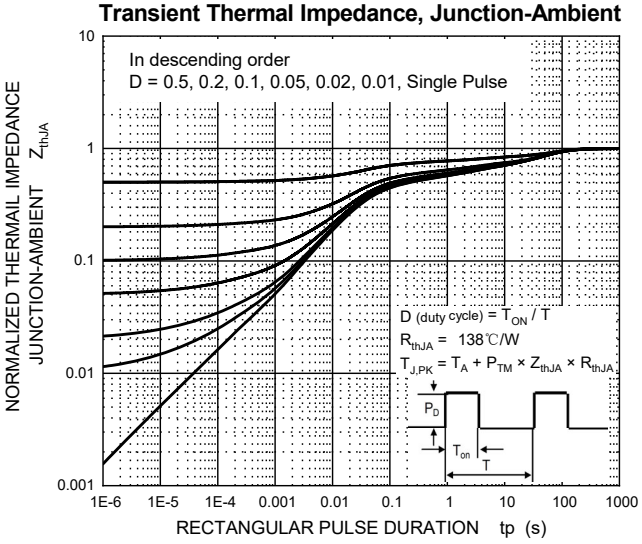
Gate Charge



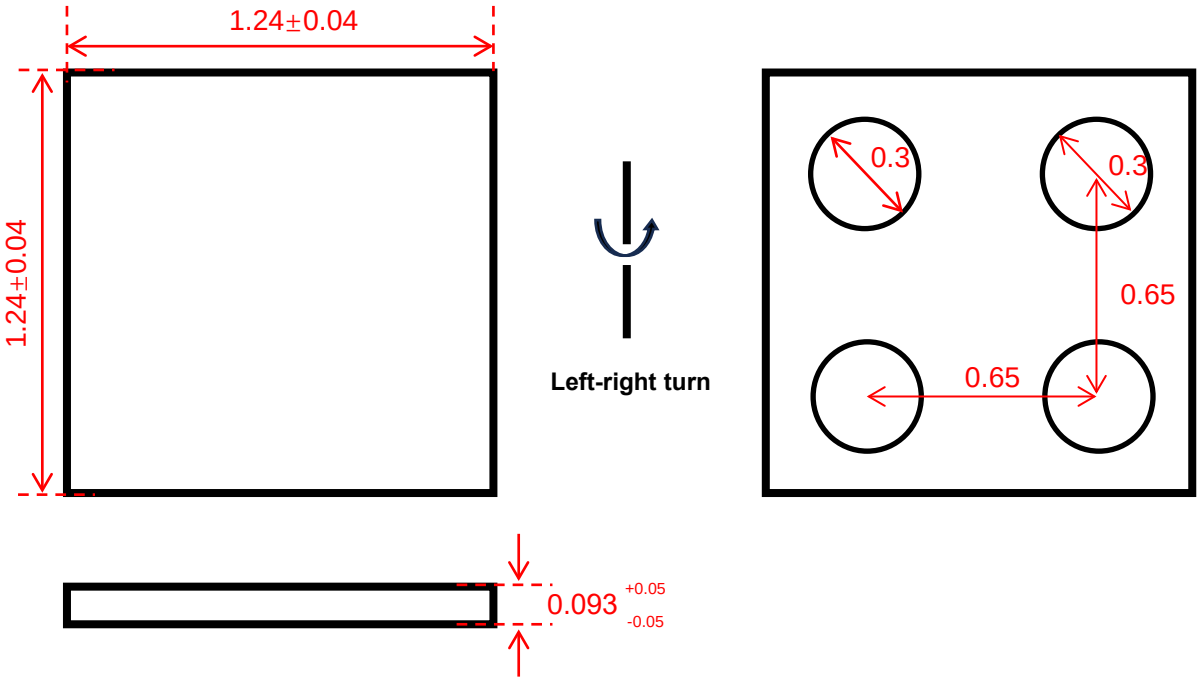
Maximum Safe Operating Area



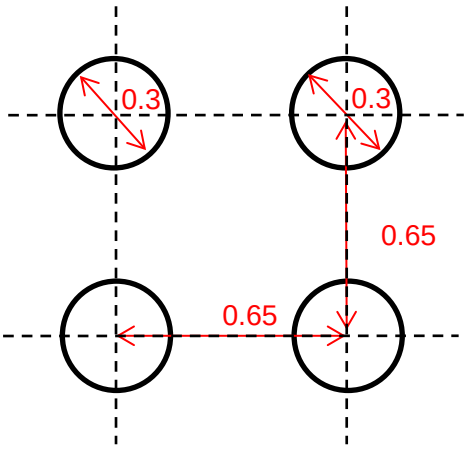
Transient Thermal Impedance, Junction-Ambient



CSPB1212-4 Package Outline Dimensions(Unit:mm)



CSPB1212-4 Suggested Pad Layout (Unit:mm)



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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